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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/783,777	02/20/2004	Wayne T. Holcombe	P1997US	6671

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EXAMINER	
BRINEY III, WALTER F	

ART UNIT	PAPER NUMBER
2646	

DATE MAILED: 11/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/783,777	HOLCOMBE ET AL.	
	Examiner	Art Unit	
	Walter F. Briney III	2646	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/22/04, 10/14/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. **Claims 1, 6-10 and 13-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hollenbach et al. (US Patent 6,205,219) in view of Talambrias (US Patent 2,977,547) and further in view of Dayton (US Patent 5,095,282).**

Claim 1 is limited to *a telephone line interface circuit*. In rejecting this claim it is noted that Hollenbach discloses a prior art call-related information receiving circuit. See figure 8. As seen in the figure, the call related information signal path includes isolation capacitors (808) and (810); a differential amplifier (820); a CODEC (830); and a DSP (840). The figure discloses that call related information signals are received from a tip and ring pair, passed across a capacitive isolation barrier that blocks DC, interfaced to an amplifier by way of linear resistors, sensed by the amplifier, converted to a digital format by a CODEC and further detected and/or processed by a DSP. It is submitted that the amplifier (820) corresponds to the differential transconductance amplifier as claimed. In particular, the amplifier (820) comprises an inverting and non-inverting input connected to a tip and ring line by way of input resistors (804) and (806). The output of the amplifier is connected to the output of the analog receiving portion, namely the CODEC (830). Note, as the term "high resistance" as used with respect to first series

and second series resistors is completely relative, and thus, is not given any patentable weight in rejecting this claim. While the circuit of figure 8 is operational, it is submitted that several elements of the claim are missing. In particular, there is no common mode canceling transconductance amplifier, no gyrator transconductance amplifier, and no capacitor coupled to a gyrator. As discussed below, however, these elements are completely conventional and provide well-known advantages to the circuit configuration of Hollenbach.

With respect to the common-mode transconductance amplifier, it is noted that Talambrias teaches a differential amplifier that is depicted in figure 1. Before proceeding, it is noted that the amplifier (820) of Hollenbach is configured in a nearly identical manner as the amplifier (14) illustrated by Talambrias. That is, both amplifiers are configured as differential receivers. In light of this, it is noted that the receiver (820) of Hollenbach is subject to the same distortion and noise problems associated with the receiver of Talambrias. In particular, the receivers are subject to loading noise sources such as common-mode sources. See column 1, lines 18-40. In solution, Talambrias includes a secondary receiver (23) configured as a common-mode receiver. This configuration is detailed in figure 2. Figure 2 indicates that the common-mode receiver (23) includes two inputs, the "inverting input" is provided at node (12) and the "non-inverting input" is depicted as the control to tube (V2). Note that node (12) is the same as the second terminal of the telephone line pair, and is connected to the non-inverting input of the differential amplifier. Further note that the input to tube V2 is connected to a voltage divider with a "first reference voltage" input. Figure 1 indicates that the

common-mode receiver includes two outputs, the "first differential output" is illustrated as the current flow path through resistor (25) toward the inverting input of the common-mode amplifier (23) while the "second differential output" is illustrated as the current flow path through resistor (24) toward the inverting input of the differential amplifier (i.e. amplifier (820) of Talambrias). It is clear that the input of the common-mode amplifier (23) does not interface to the second terminal of the telephone line pair through the same resistor (18) as the differential amplifier (14). However, for the purposes of this rejection, the source resistances (7) and (8) will be considered as the "first and second series of high resistance value resistors."

It would have been obvious to one of ordinary skill in the art at the time of the invention to include a common-mode receiver as taught by Talambrias for the purpose of removing common-mode noise interference at the output of a differential amplifier.

With respect to the gyrator transconductance amplifier, it is noted that Dayton teaches a differential amplifier apparatus that is depicted in figure 3. Dayton teaches that using balanced isolation capacitors, such as capacitors (808) and (810) used by Hollenbach significantly increase the chance that the circuit will malfunction. Specifically, the two capacitors (808) and (810) must be matched almost perfectly to each other because any deviation can significantly reduce common-mode noise tolerance. See column 4, lines 50-57. In solution, Dayton provides a DC feedback circuit comprising amplifier (A5) and capacitor (C2). As can be seen from figure 3, the "inverting input" of the amplifier (A5) is connected to a single-ended output of the differential amplifier, where the output is indicated as the current flow path through

resistor (R17). The "non-inverting input" of the amplifier (A5) is connected to a "second reference voltage." The "first differential output" of the DC feedback amplifier is illustrated as the current flow path through resistor (R15) and is connected to the non-inverting input of the differential amplifier, which is connected to the inverting input of the common-mode amplifier as illustrated in figures 1 and 2 of Talambrias, while the "second differential output" is illustrated as the current flow path through the capacitor (C2) towards the output terminal of the circuit. The "capacitor" (C2) is coupled between the inverting input of the DC cancelling amplifier and a power supply terminal connected to one end of resistor (R14).

It would have been obvious to one of ordinary skill in the art at the time of the invention to include a DC cancelling amplifier as taught by Dayton for the purpose of removing DC without lowering common-mode noise tolerance.

Claim 6 is limited to *the circuit of claim 1*, as covered by Hollenbach in view of Talambrias and further in view of Dayton. It is noted that none of the above mentioned prior art references make reference to integrating each component into an integrated circuit excluding the capacitor as taught by Dayton. As discussed below, however, this procedure is completely conventional and provides well-known advantage to the circuit configuration of Hollenbach in view of Talambrias and further in view of Dayton.

The examiner takes Official Notice of the fact that it was well known to integrate electronic circuits with a common purpose into an integrated circuit with the exception of certain components that are regarded as too big or bulky to be integrated, e.g. capacitors with a cut-off within the voice range of a telephone. It would have been

obvious to one of ordinary skill in the art at the time of the invention to integrate the transistor-based amplifiers that comprise the differential amplifier, common-mode amplifier, and DC feedback amplifier taught by the prior art while providing an external connection to a bulky capacitor as was known in the prior art for the purpose of mass producing the resulting call-related information interface circuits and reducing the overall size of the interface circuits.

Claim 7 is limited to *the circuit of claim 1*, as covered by Hollenbach in view of Talambrias and further in view of Dayton. It is noted that none of the above mentioned prior art references make reference to the type of resistors used in the interface circuits, let alone the use of 1% tolerance resistors. As discussed below, however, use of these elements is completely conventional and provides well-known advantage to the circuit configuration of Hollenbach in view of Talambrias and further in view of Dayton.

The examiner takes Official Notice of the fact that it was well known to use 1% tolerance resistors. It would have been obvious to one of ordinary skill in the art at the time of the invention to use 1% tolerance resistors as was known in the prior art for the purpose of reducing differences in resistances, and thus, producing circuits that behave more closely to their design.

Claim 8 is limited to *a method for interfacing to a telephone line*. As discussed supra apropos the rejection of claim 1, Hollenbach in view of Talambrias and further in view of Dayton make obvious a call-related information signal differential amplifier (as disclosed by Hollenbach) with a common mode cancelling amplifier (as taught by Talambrias) and a DC cancelling amplifier (as taught by Dayton). Furthermore, all steps

of this method are inherently performed by the combination discussed in the rejection of claim 1. Therefore, Hollenbach in view of Talambrias and further in view of Dayton makes obvious all limitations of the claim.

Claim 9 is limited to *the method of claim 8*, as covered by Hollenbach in view of Talambrias and further in view of Dayton. Dayton teaches using a capacitor (C2) to eliminate DC signals. Therefore, Hollenbach in view of Talambrias and further in view of Dayton makes obvious all limitations of the claim.

Claim 10 is limited to *the method of claim 8*, as covered by Hollenbach in view of Talambrias and further in view of Dayton. Dayton teaches providing a DC signal at the output of amplifier (A5) and providing a pure differential signal at the output of (A4). The output of (A4) corresponds to the output of (820) as disclosed by Hollenbach. This signal is a call-ID signal, i.e. a "polarity signal." Therefore, Hollenbach in view of Talambrias and further in view of Dayton makes obvious all limitations of the claim.

Claim 13 is limited to *the method of claim 8*, as covered by Hollenbach in view of Talambrias and further in view of Dayton. As seen in figure 8 of Hollenbach, the output of the differential amplifier (820) is looped back to the input to cancel an input at circuit node R. Therefore, Hollenbach in view of Talambrias and further in view of Dayton makes obvious all limitations of the claim.

Claim 14 is limited to *the method of claim 8*, as covered by Hollenbach in view of Talambrias and further in view of Dayton. As noted in the rejection of claim 1, the operation of the common-mode cancelling circuit taught by Talambrias inherently

performs the operations recited in this claim. Therefore, Hollenbach in view of Talambrias and further in view of Dayton makes obvious all limitations of the claim.

Claim 15 is limited to *the method of claim 8*, as covered by Hollenbach in view of Talambrias and further in view of Dayton. The circuit made obvious by Hollenbach in view of Talambrias and Dayton includes inputs to a telephone line that can be represented as a network of high resistance value resistors, where the limitation "high resistance" is completely relative, and thus, given no patentable weight. Therefore, Hollenbach in view of Talambrias and further in view of Dayton makes obvious all limitations of the claim.

Claim 16 is limited to *the method of claim 8*, as covered by Hollenbach in view of Talambrias and further in view of Dayton. The common-mode amplifier (23) of Talambrias, like any operational amplifier, can be regarded as a transconductance amplifier. Therefore, Hollenbach in view of Talambrias and further in view of Dayton makes obvious all limitations of the claim.

Claim 17 is limited to *the method of claim 8*, as covered by Hollenbach in view of Talambrias and further in view of Dayton. The differential amplifier (820) of Hollenbach, like any operational amplifier, can be regarded as a transconductance amplifier. Therefore, Hollenbach in view of Talambrias and further in view of Dayton makes obvious all limitations of the claim.

Claim 18 is limited to *the method of claim 8*, as covered by Hollenbach in view of Talambrias and further in view of Dayton. The DC amplifier (A5) of Dayton, like any operational amplifier, can be regarded as a transconductance amplifier. Therefore,

Hollenbach in view of Talambrias and further in view of Dayton makes obvious all limitations of the claim.

Claim 19 is limited to *the method of claim 8*, as covered by Hollenbach in view of Talambrias and further in view of Dayton. Hollenbach discloses using a CODEC (830) to convert the differential call related information signal into call-ID data. See column 1, line 66, through column 2, line 8. Therefore, Hollenbach in view of Talambrias and further in view of Dayton makes obvious all limitations of the claim.

Claim 20 is limited to *the method of claim 8*, as covered by Hollenbach in view of Talambrias and further in view of Dayton. Hollenbach discloses using a CODEC (830) to convert the differential call related information signal into call-ID data. See column 1, line 66, through column 2, line 8. Therefore, Hollenbach in view of Talambrias and further in view of Dayton makes obvious all limitations of the claim.

Claim 21 is limited to *a telephone line interface device*. As shown in the rejection of claim 1, Hollenbach in view of Talambrias and further in view of Dayton makes obvious a telephone line interface with a "high resistance interface" including source resistances (7) and (8) as depicted in figure 1 of Talambrias; a common mode cancelling transconductance amplifying means (23) as depicted in figure 1 of Talambrias; a differential transconductance amplifying means (820) as depicted in figure 8 of Hollenbach; and a gyrator transconductance amplifying means (A5) as depicted in figure 3 of Dayton. Therefore, Hollenbach in view of Talambrias and further in view of Dayton makes obvious all limitations of the claim.

Claim 22 is limited to *the device of claim 21*, as covered by Hollenbach in view of Talambrias and further in view of Dayton. As seen in the various figures of the cited prior art, "biasing means" are needed. The recitation "low noise" is completely relative, and thus, is given no patentable weight. Therefore, Hollenbach in view of Talambrias and further in view of Dayton makes obvious all limitations of the claim.

2. **Claims 2, 3, 11, 12, 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hollenbach in view of Talambrias in view of Dayton and further in view of Smith (US Patent 4,292,595).**

Claim 2 is limited to *the circuit of claim 1*, as covered by Hollenbach in view of Talambrias and further in view of Dayton. It is noted that beyond indicating the presence of CODEC (830), there is no indication that the CODEC encodes the received call related information signals using pulse width modulation. As discussed below, however, this element is completely conventional and provides well-known advantages to the circuit configuration of Hollenbach.

With respect to the PWM analog-to-digital converter as recited, it is noted that Smith teaches a capacitance coupled isolation amplifier and method as depicted in figure 1. The device of Smith provides PWM conversion with the further advantage of reduced cost over prior art converters and increased sensitivity to EMI. See column 1, line 56, through column 2, line 34.

It would have been obvious to one of ordinary skill in the art at the time of the invention to convert received analog call related information signals into a digital format using a PWM converter as taught by Smith for the purpose of providing a low cost

converter with low EMI sensitivity. Furthermore, because Hollenbach does not dictate the exact type of CODEC to use, it is submitted that one of ordinary skill in the art at the time of the invention would have been inherently motivated to use a known CODEC configuration.

Claim 3 is limited to *the circuit of claim 2*, as covered by Hollenbach in view of Talambrias further in view of Dayton and further in view of Smith. The PWM converter of Smith includes a "control circuit" comprising elements of block (3) and elements of block (7) as depicted in figure 1. Clock signals (47) and (49) as well as control signals (44) and (45) are generated in response to a "reference clock" comprising amplifier (17). In response, a "comparison signal" is generated by way of "PWM conversion circuitry" comprising transistors (63) and (66). A "PWM encoded signal" is generated by the control circuit further comprising transistors (75) and (77) in response to the comparison signal generated by transistors (63) and (66) of the PWM conversion circuitry. Therefore, Hollenbach in view of Talambrias in view of Dayton and further in view of Smith makes obvious all limitations of the claim.

Claim 11 recites essentially the same limitations as claim 2, as covered by Hollenbach in view of Talambrias in view of Dayton and further in view of Smith, and is rejected for the same reasons.

Claim 12 recites essentially the same limitations as claim 2, as covered by Hollenbach in view of Talambrias in view of Dayton and further in view of Smith, and is rejected for the same reasons.

Claim 23 recites essentially the same limitations as claim 2, as covered by Hollenbach in view of Talambrias in view of Dayton and further in view of Smith, and is rejected for the same reasons.

Claim 24 recites essentially the same limitations as claim 3, as covered by Hollenbach in view of Talambrias in view of Dayton and further in view of Smith, and is rejected for the same reasons.

Allowable Subject Matter

The following is a statement of reasons for the indication of allowable subject matter:

3. **Claims 4 and 5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.**

Claim 4 is limited to *the circuit of claim 1*, as covered by Hollenbach in view of Talambrias and further in view of Dayton.

Claim 5 is limited to *the circuit of claim 4*, as covered by Hollenbach in view of Talambrias and further in view of Dayton. Because claim 5 is dependent on claim 4, it is allowable over the cited prior art for at least the same reasons.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter F. Briney III whose telephone number is 571-272-7513. The examiner can normally be reached on M-F 8am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh Tran can be reached on 571-272-7564. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SINH TRAN
SUPERVISORY PATENT EXAMINER

WFB
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